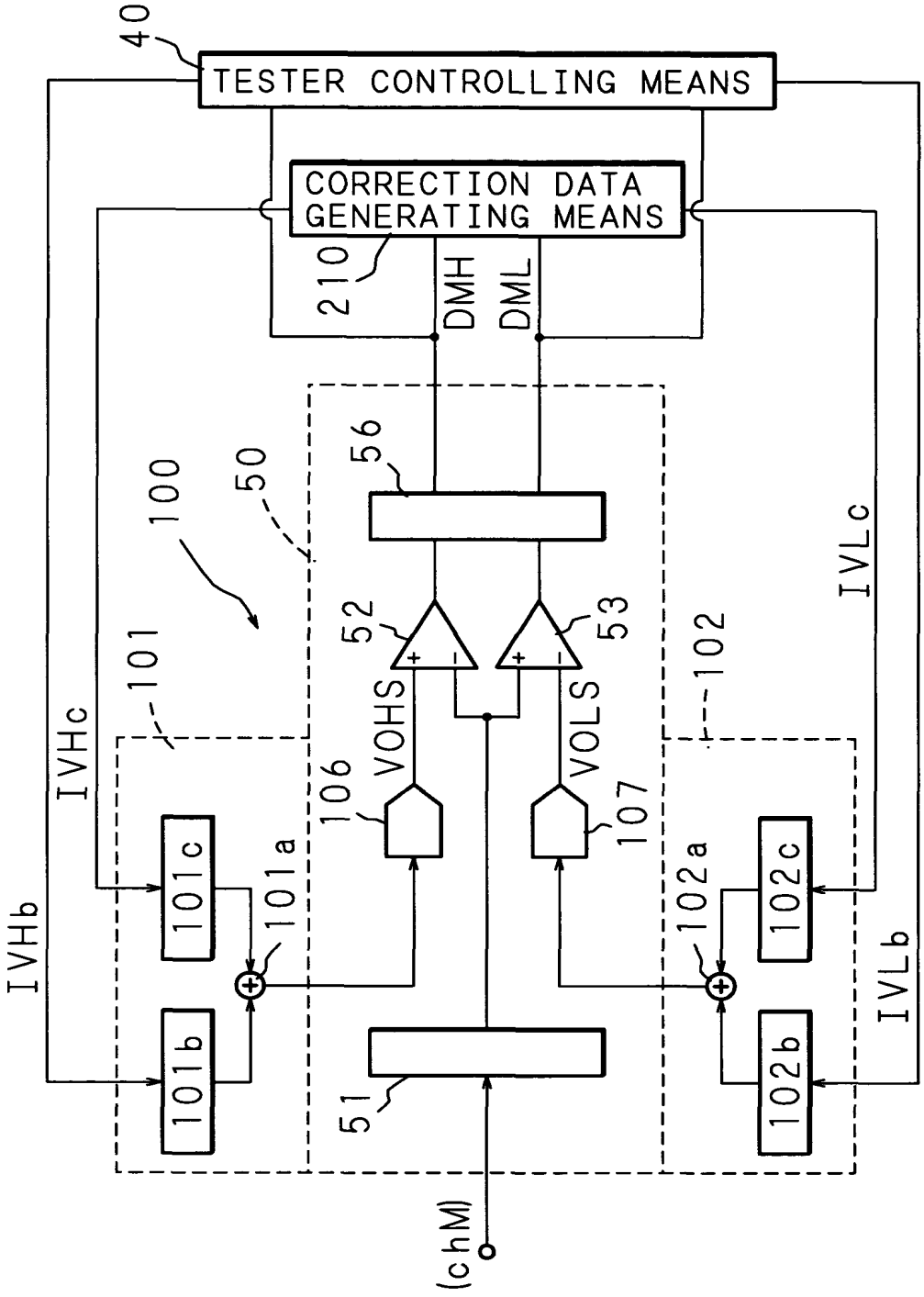

40
TESTER CONTROLLING MEANS
CORRECTION DATA GENERATING MEANS
210
DMH
DML
56
100
50
52
53
101
102
IVHc
IVLc
VOHS
VOLS
106
107
101c
101a
102a
102c
IVHb
IVLb
101b
102b
51
(chM)

FIG. 1

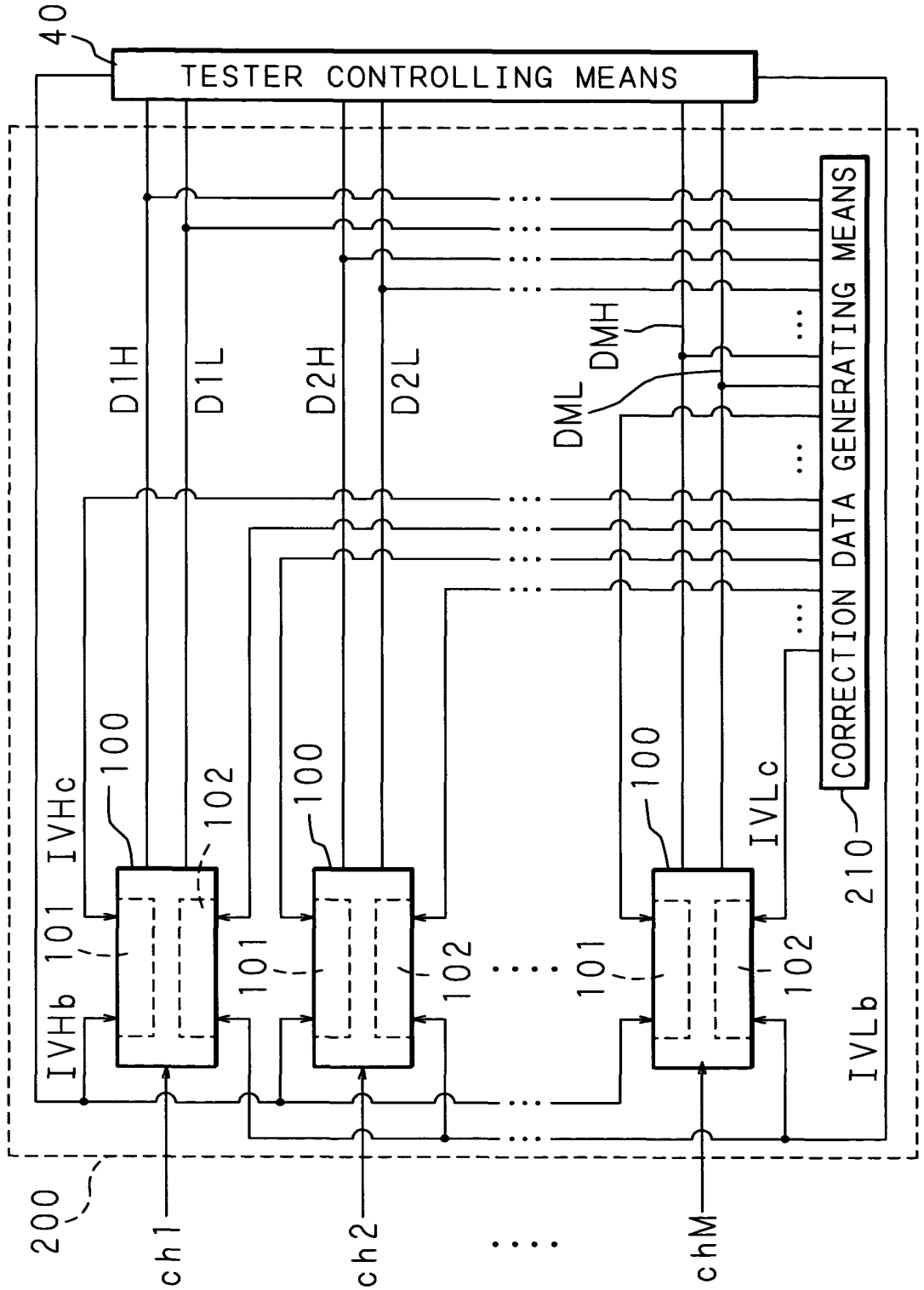
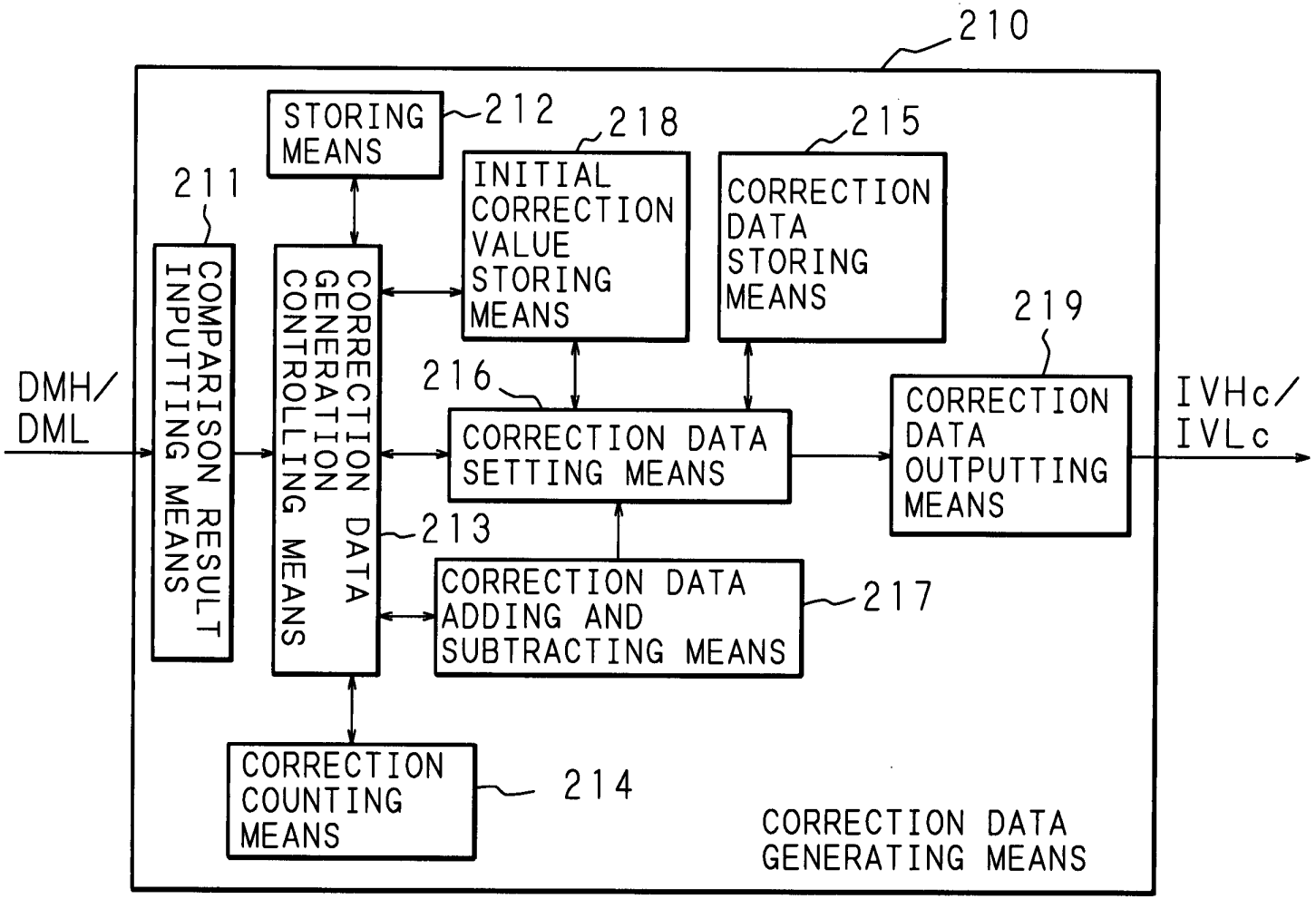

40
TESTER CONTROLLING MEANS
D1H
D1L
D2H
D2L
DMH
DML
CORRECTION DATA GENERATING MEANS
210
IVHc
IVHb
IVLc
IVLb
100
101
102
200
ch1
ch2
chM

FIG. 2

FIG. 3


210
STORING MEANS
212
218
215
211
INITIAL CORRECTION VALUE STORING MEANS
CORRECTION DATA STORING MEANS
219
DMH/ DML
COMPARISON RESULT INPUTTING MEANS
CORRECTION DATA GENERATION CONTROLLING MEANS
216
CORRECTION DATA SETTING MEANS
CORRECTION DATA OUTPUTTING MEANS
IVHc/ IVLc
213
CORRECTION DATA ADDING AND SUBTRACTING MEANS
217
CORRECTION COUNTING MEANS
214
CORRECTION DATA GENERATING MEANS

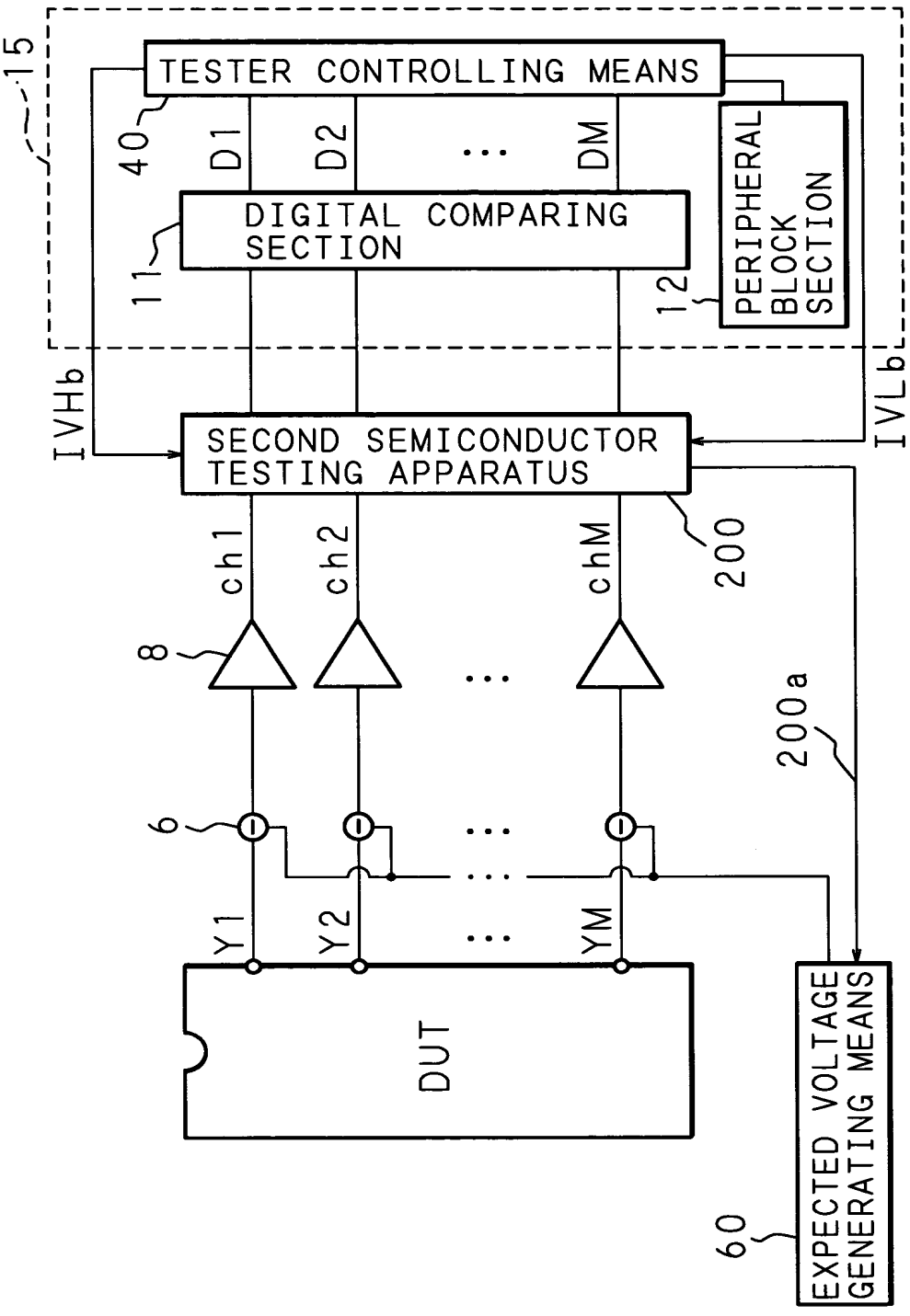

15
TESTER CONTROLLING MEANS
40
D1
D2
DM
DIGITAL COMPARING SECTION
11
12
PERIPHERAL BLOCK SECTION
IVHb
IVLb
SECOND SEMICONDUCTOR TESTING APPARATUS
200
ch1
ch2
chM
8
200a
6
Y1
Y2
YM
DUT
60
EXPECTED VOLTAGE GENERATING MEANS

FIG. 4

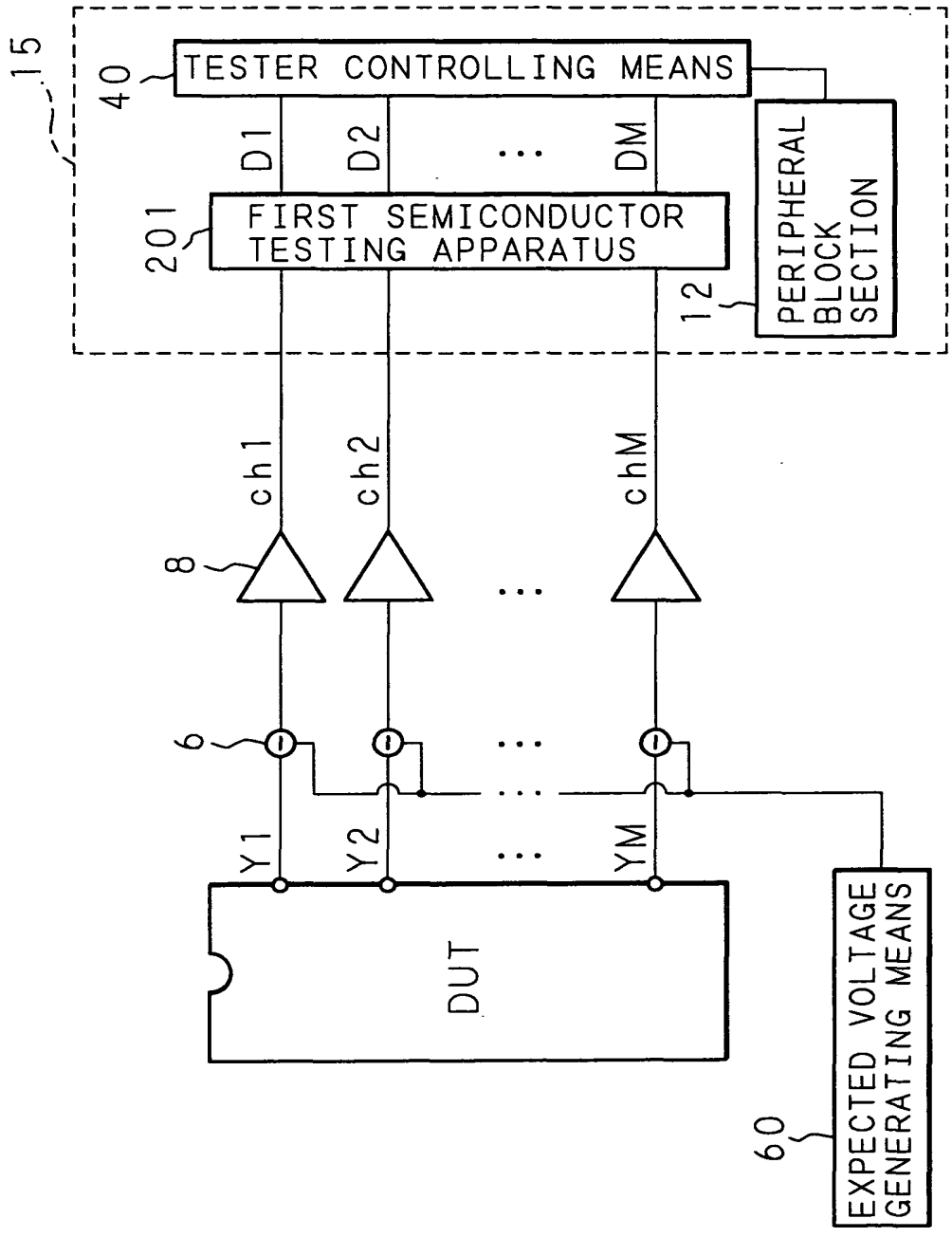

15
40
TESTER CONTROLLING MEANS
D1
D2
DM
201
FIRST SEMICONDUCTOR TESTING APPARATUS
12
PERIPHERAL BLOCK SECTION
ch1
ch2
chM
8
6
Y1
Y2
YM
DUT
60
EXPECTED VOLTAGE GENERATING MEANS

FIG. 5

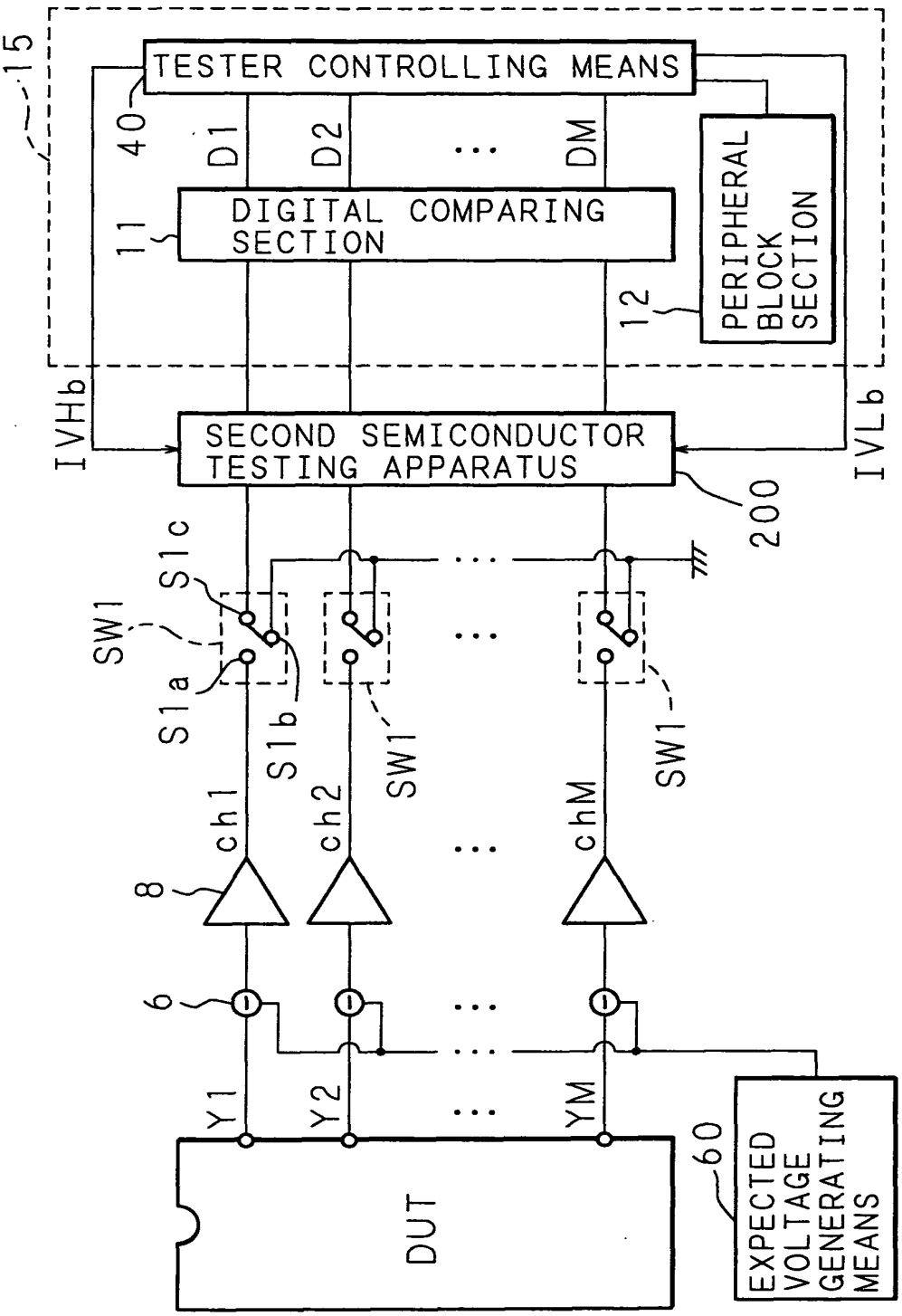

15
TESTER CONTROLLING MEANS
40
D1
D2
DM
DIGITAL COMPARING SECTION
11
PERIPHERAL BLOCK SECTION
12
IVHb
IVLb
SECOND SEMICONDUCTOR TESTING APPARATUS
200
SW1
S1c
S1a
S1b
ch1
ch2
chM
8
6
Y1
Y2
YM
DUT
60
EXPECTED VOLTAGE GENERATING MEANS

FIG. 6

FIG. 7

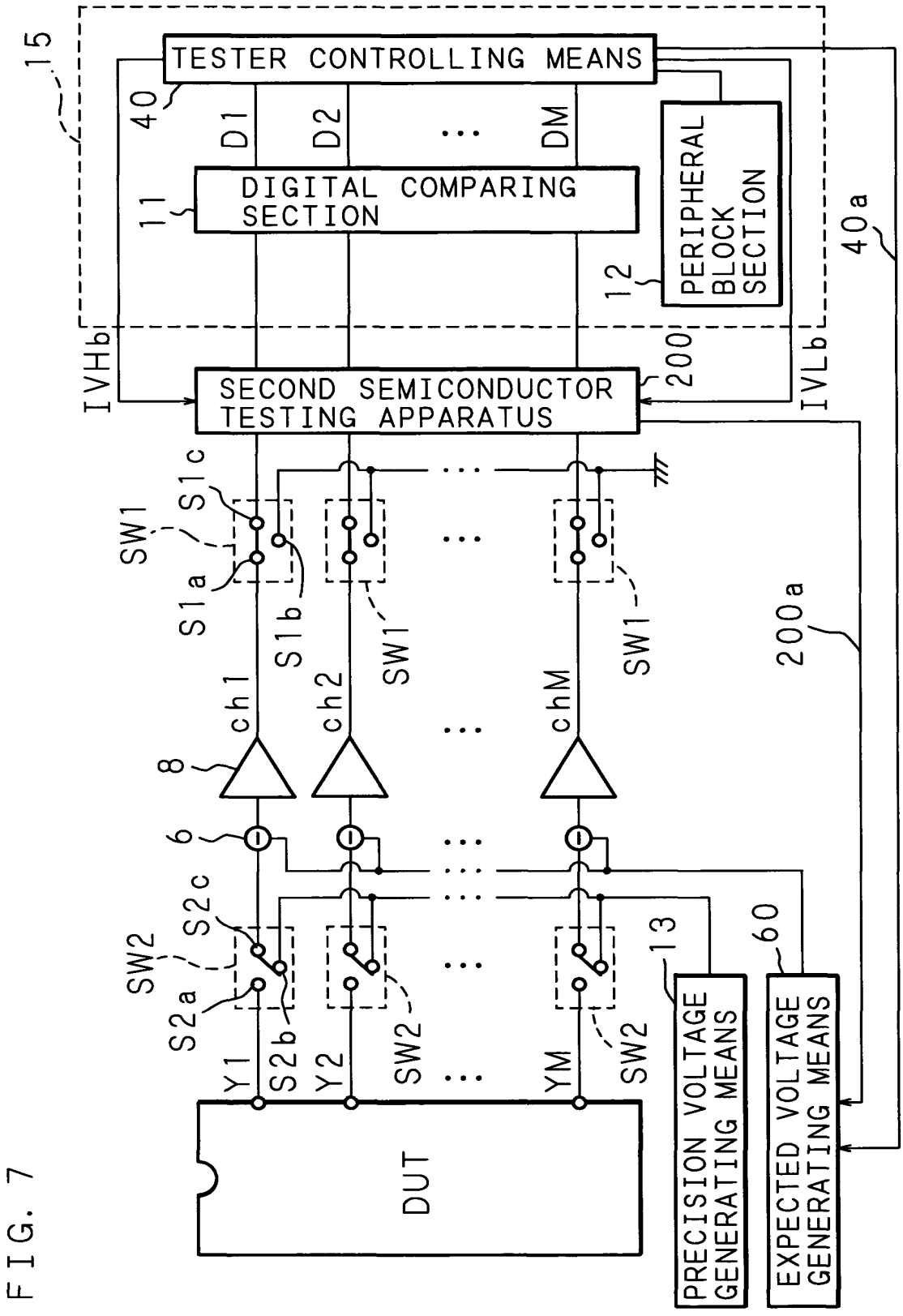

15
TESTER CONTROLLING MEANS
40
D1
D2
DM
DIGITAL COMPARING SECTION
11
PERIPHERAL BLOCK SECTION
12
40a
IVHb
IVLb
200
SECOND SEMICONDUCTOR TESTING APPARATUS
SW1
S1c
S1a
S1b
ch1
ch2
chM
200a
8
6
SW2
S2c
S2a
S2b
Y1
Y2
YM
DUT
13
60
PRECISION VOLTAGE GENERATING MEANS
EXPECTED VOLTAGE GENERATING MEANS

FIG. 8

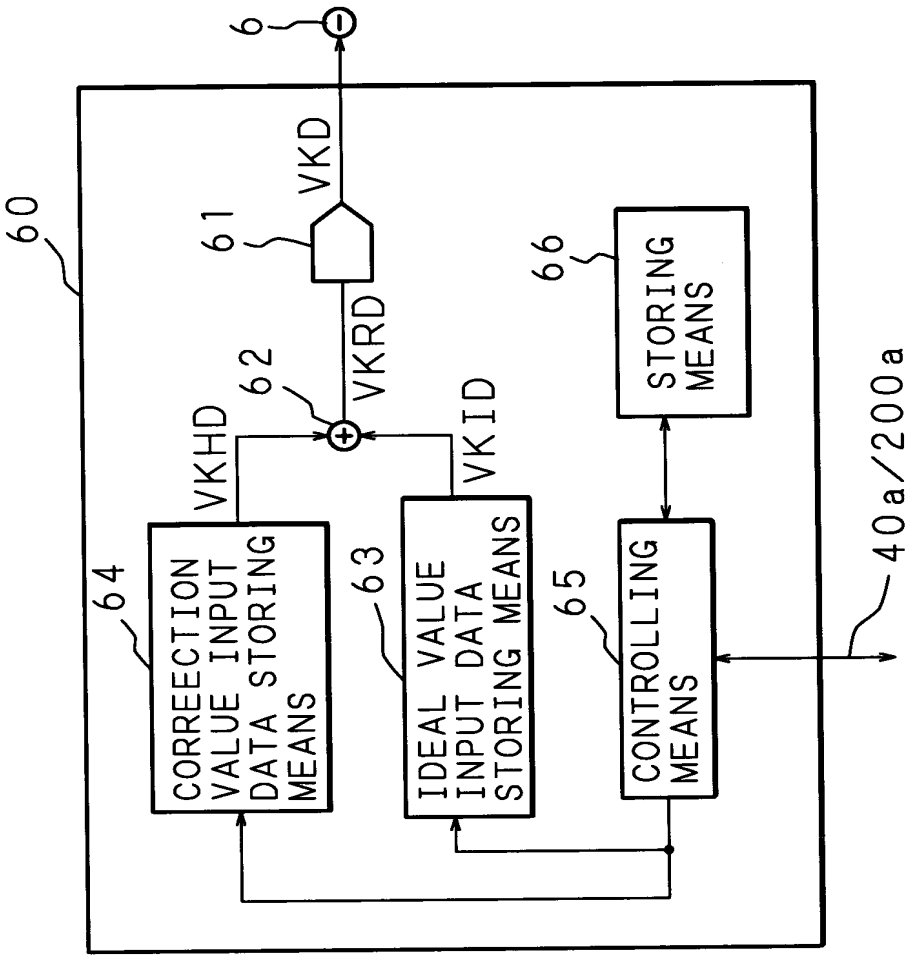

6
60
61
VKD
VKRD
62
VKHD
VKID
64
CORRECTION VALUE INPUT DATA STORING MEANS
63
IDEAL VALUE INPUT DATA STORING MEANS
65
CONTROLLING MEANS
66
STORING MEANS
40a/200a

FIG. 9

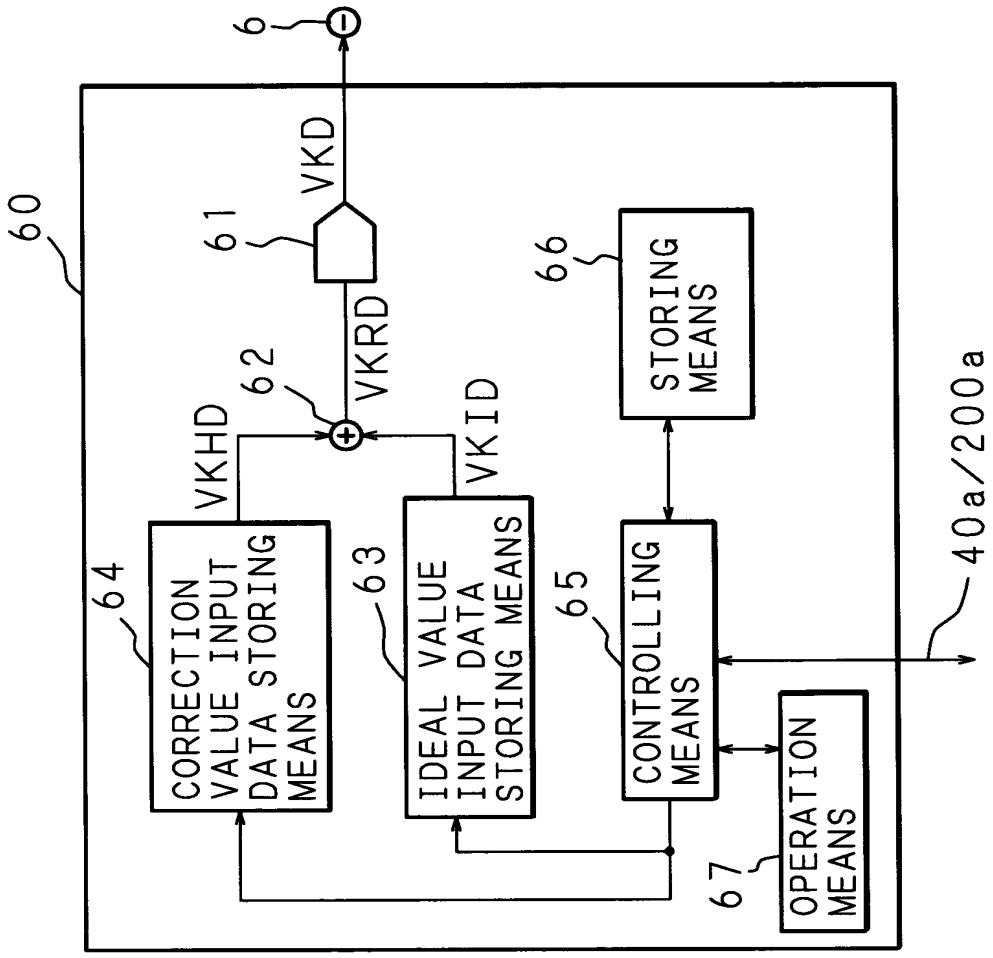

60
6
VKD
61
VKRD
62
VKHD
VKID
64
CORRECTION VALUE INPUT DATA STORING MEANS
63
IDEAL VALUE INPUT DATA STORING MEANS
65
CONTROLLING MEANS
66
STORING MEANS
67
OPERATION MEANS
40a/200a

FIG. 10

(UNIT:mV)

STEP	IVHc CORRECTION VALUE	POSITIVE TERMINAL INPUT VOLTAGE (EFFECTIVE INPUT VOLTAGE)	COMPARATOR OUTPUT	ERROR
1	128	148	HIGH	148
2	−64	−44	LOW	−44
3	32	52	HIGH	52
4	−16	4	HIGH	4
5	−40	−20	LOW	−20
6	−28	−8	LOW	−8
7	−22	−2	LOW	−2
8	−19	1	HIGH	1
9	−20.5	−0.5	LOW	−0.5
10	−19.75	0.25	HIGH	0.25
11	−20.125	−0.125	LOW	−0.125
12	−19.9375	0.0625	HIGH	0.0625

(DAC QUANTIZATION ERROR:REMOVED)

FIG. 11

(UNIT:mV)

STEP	IVHc CORRECTION VALUE	POSITIVE TERMINAL INPUT VOLTAGE (EFFECTIVE INPUT VOLTAGE)	COMPARATOR OUTPUT	ERROR
21	−128	−118	LOW	148
22	64	74	HIGH	−44
23	−32	−22	LOW	52
24	16	6	HIGH	4
25	−8	2	HIGH	−20
26	−20	−10	LOW	−8
27	−14	−4	LOW	−2
28	−11	−1	LOW	1
29	−9.5	0.5	HIGH	−0.5
30	−10.25	−0.25	LOW	−0.25
31	−9.875	0.125	HIGH	0.125
32	−10.0625	−0.0625	LOW	−0.0675

(DAC QUANTIZATION ERROR:REMOVED)

FIG. 12

(UNIT : mV)

STEP	DAC				AMPLIFIER		COMPARATOR OUTPUT VOLTAGE
	IDEAL INPUT DATA VKID	CORRECTION INPUT DATA VKHD	REAL INPUT DATA VKRD	EFFECTIVE OUTPUT VOLTAGE VKD	INPUT VOLTAGE	OUTPUT VOLTAGE	
41	100	128	228	218	-118	-2832	LOW
42	100	-64	36	26	74	1776	HIGH
43	100	32	132	122	-22	-528	LOW
44	100	-16	84	74	26	624	HIGH
45	100	8	108	98	2	48	HIGH
46	100	20	120	110	-10	-240	LOW
47	100	14	114	104	-4	-96	LOW
48	100	11	111	101	-1	-24	LOW
49	100	9.5	109.5	99.5	0.5	12	HIGH
50	100	10.25	110.25	100.25	-0.25	-6	LOW
51	100	9.875	109.875	99.875	0.125	3	HIGH
52	100	10.0625	110.0625	100.0625	-0.0625	-1.5	LOW
53	100	9.9688	109.9688	99.9688	0.0312	0.7488	HIGH
54	100	10.015675	110.015675	100.015675	-0.015675	-0.3762	LOW
55	100	9.992237	109.992237	99.992237	0.00777	0.1865	HIGH

(OUTPUT VOLTAGE OF PRECISION VOLTAGE GENERATING MEANS13=100mV (FIXED))

FIG. 13

(UNIT : mV)

STEP	DAC				AMPLIFIER		COMPARATOR OUTPUT VOLTAGE	VKS
	IDEAL INPUT DATA VKID	CORRECTION INPUT DATA VKHD	REAL INPUT DATA VKRD	EFFECTIVE OUTPUT VOLTAGE VKD	INPUT VOLTAGE	OUTPUT VOLTAGE		
61	100	128	228	228.023	-128.023	-3072.552	LOW	100
62	100	-64	36	36.004	63.996	1535.904	HIGH	100
63	100	32	132	132.013	-32.013	-768.312	LOW	100
64	100	-16	84	84.008	15.992	383.808	HIGH	100
65	100	8	108	108.011	-8.011	-192.264	LOW	100
66	100	-4	96	96.010	3.990	95.760	HIGH	100
67	100	2	102	102.010	-2.010	-48.240	LOW	100
68	100	-1	99	99.010	0.990	23.760	HIGH	100
69	100	0.5	100.5	105.510	-0.510	-12.240	LOW	100
70	100	-0.25	99.75	99.760	0.240	5.760	HIGH	100
71	100	0.125	100.125	100.135	-0.135	-3.240	LOW	100
72	100	-0.0625	99.9375	99.947	-0.053	1.272	HIGH	100

(OUTPUT VOLTAGE VKS OF PRECISION VOLTAGE GENERATING MEANS13=100mV (FIXED))

FIG. 14

(UNIT: mV)

STEP	DAC				AMPLIFIER		COMPARATOR OUTPUT VOLTAGE	
	IDEAL INPUT DATA VKID	CORRECTION INPUT DATA VKHD	REAL INPUT DATA VKRD	EFFECTIVE OUTPUT VOLTAGE VKD	INPUT VOLTAGE	OUTPUT VOLTAGE		VKS
81	12900	-128	12772	12773.277	126.723	3041.352	LOW	12900
82	12900	64	12964	12965.296	-65.296	-1567.104	HIGH	12900
83	12900	-32	12868	12869.287	30.723	737.112	LOW	12900
84	12900	16	12916	12917.292	-17.292	-415.008	HIGH	12900
85	12900	-8	12892	12893.289	6.711	162.064	LOW	12900
86	12900	4	12904	12905.290	-5.290	-126.960	HIGH	12900
87	12900	-2	12898	12899.290	0.710	17.040	LOW	12900
88	12900	1	12901	12902.290	-2.290	-54.960	HIGH	12900
89	12900	-0.5	12899.5	12900.790	-0.790	-18.960	HIGH	12900
90	12900	-1.25	12898.75	12900.040	-0.040	-0.960	HIGH	12900
91	12900	-1.625	12898.375	12899.665	0.335	8.040	LOW	12900
92	12900	-1.4375	12898.563	12899.852	0.148	3.552	LOW	12900

(OUTPUT VOLTAGE VKS OF PRECISION VOLTAGE GENERATING MEANS13=12900mV (FIXED))

FIG. 15

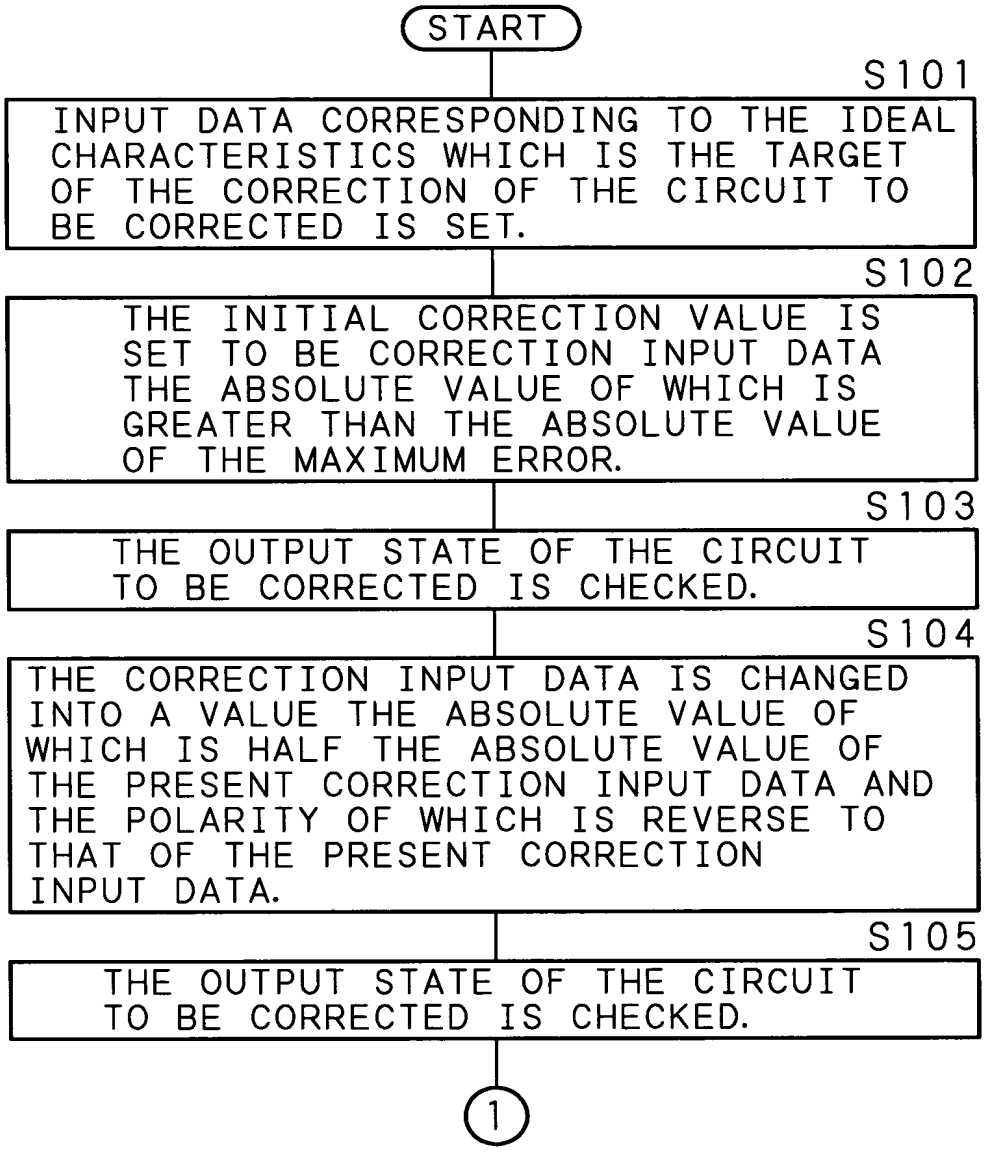

START
S101
INPUT DATA CORRESPONDING TO THE IDEAL CHARACTERISTICS WHICH IS THE TARGET OF THE CORRECTION OF THE CIRCUIT TO BE CORRECTED IS SET.
S102
THE INITIAL CORRECTION VALUE IS SET TO BE CORRECTION INPUT DATA THE ABSOLUTE VALUE OF WHICH IS GREATER THAN THE ABSOLUTE VALUE OF THE MAXIMUM ERROR.
S103
THE OUTPUT STATE OF THE CIRCUIT TO BE CORRECTED IS CHECKED.
S104
THE CORRECTION INPUT DATA IS CHANGED INTO A VALUE THE ABSOLUTE VALUE OF WHICH IS HALF THE ABSOLUTE VALUE OF THE PRESENT CORRECTION INPUT DATA AND THE POLARITY OF WHICH IS REVERSE TO THAT OF THE PRESENT CORRECTION INPUT DATA.
S105
THE OUTPUT STATE OF THE CIRCUIT TO BE CORRECTED IS CHECKED.
1

FIG. 16A

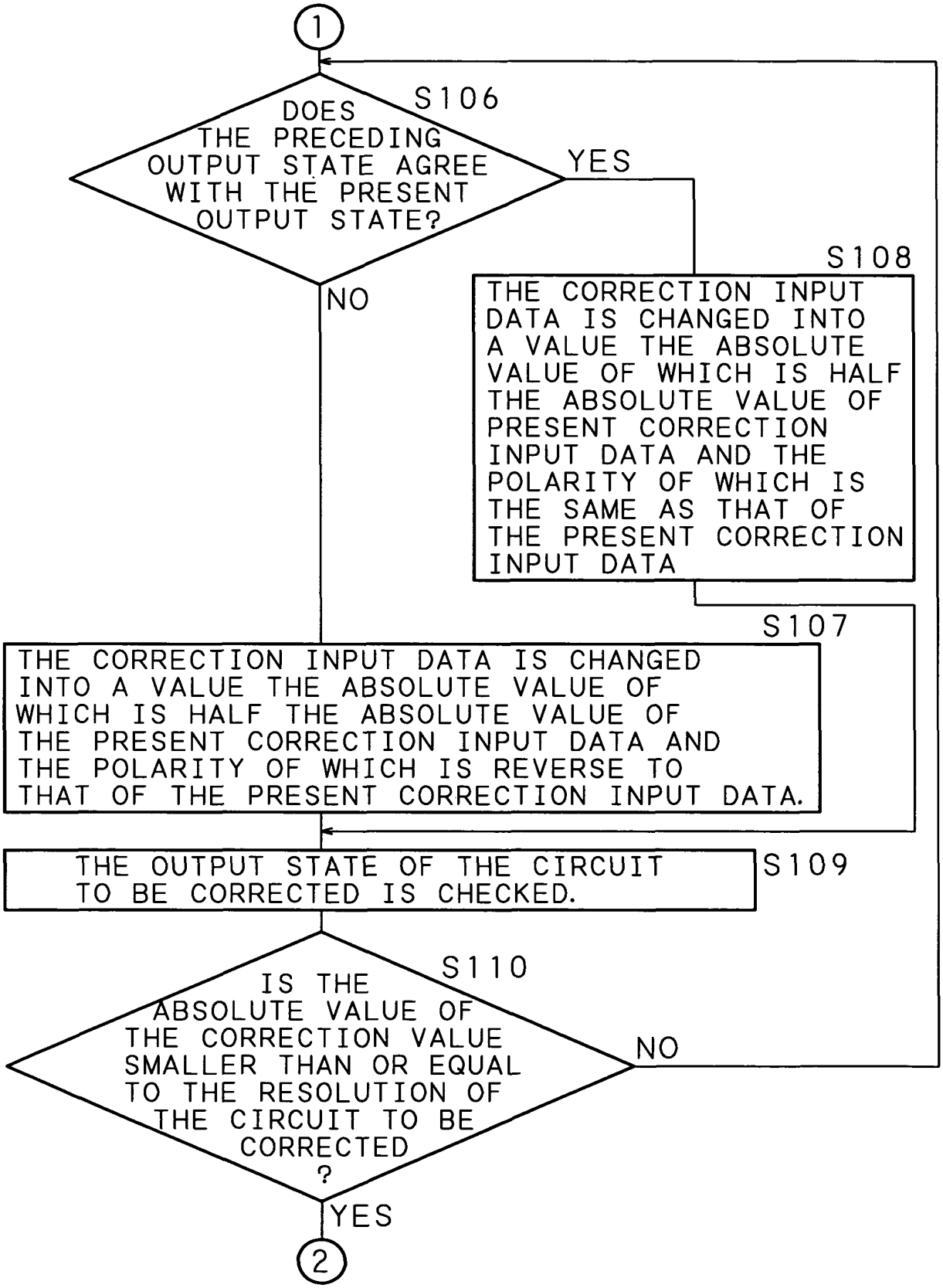

1
S106
DOES THE PRECEDING OUTPUT STATE AGREE WITH THE PRESENT OUTPUT STATE?
YES
NO
S108
THE CORRECTION INPUT DATA IS CHANGED INTO A VALUE THE ABSOLUTE VALUE OF WHICH IS HALF THE ABSOLUTE VALUE OF PRESENT CORRECTION INPUT DATA AND THE POLARITY OF WHICH IS THE SAME AS THAT OF THE PRESENT CORRECTION INPUT DATA
S107
THE CORRECTION INPUT DATA IS CHANGED INTO A VALUE THE ABSOLUTE VALUE OF WHICH IS HALF THE ABSOLUTE VALUE OF THE PRESENT CORRECTION INPUT DATA AND THE POLARITY OF WHICH IS REVERSE TO THAT OF THE PRESENT CORRECTION INPUT DATA.
THE OUTPUT STATE OF THE CIRCUIT TO BE CORRECTED IS CHECKED.
S109
S110
IS THE ABSOLUTE VALUE OF THE CORRECTION VALUE SMALLER THAN OR EQUAL TO THE RESOLUTION OF THE CIRCUIT TO BE CORRECTED ?
NO
YES
2

FIG. 16B

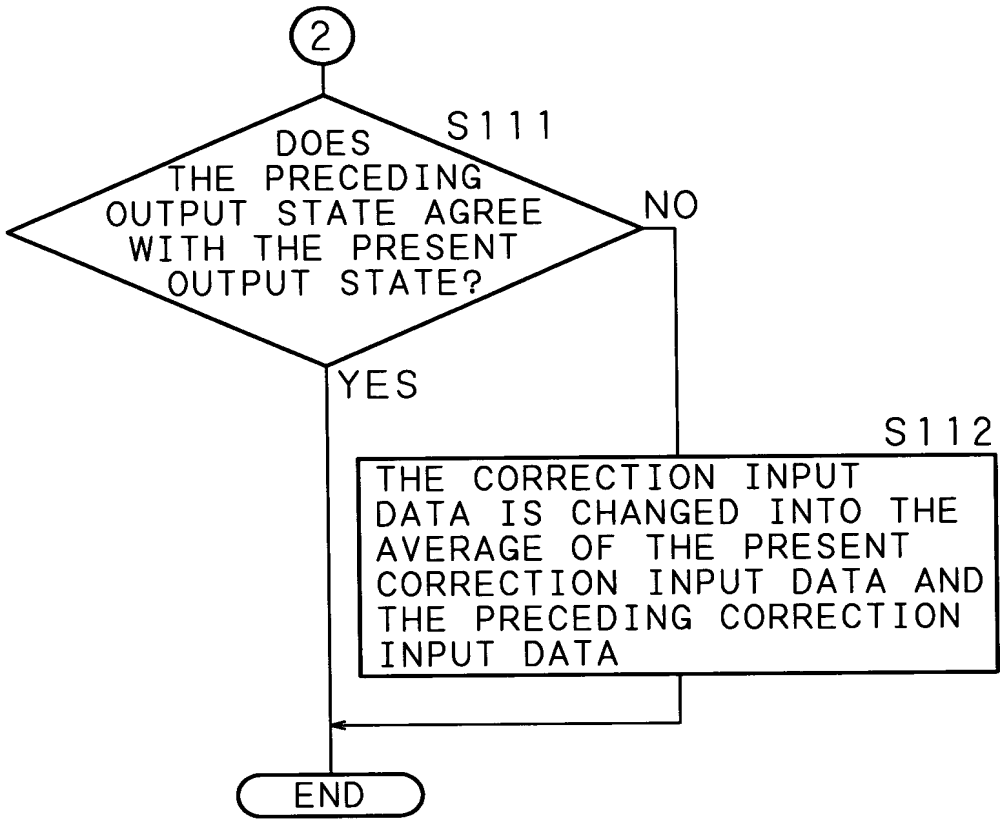

2
S111
DOES THE PRECEDING OUTPUT STATE AGREE WITH THE PRESENT OUTPUT STATE?
NO
YES
S112
THE CORRECTION INPUT DATA IS CHANGED INTO THE AVERAGE OF THE PRESENT CORRECTION INPUT DATA AND THE PRECEDING CORRECTION INPUT DATA
END

FIG. 17
PRIOR ART

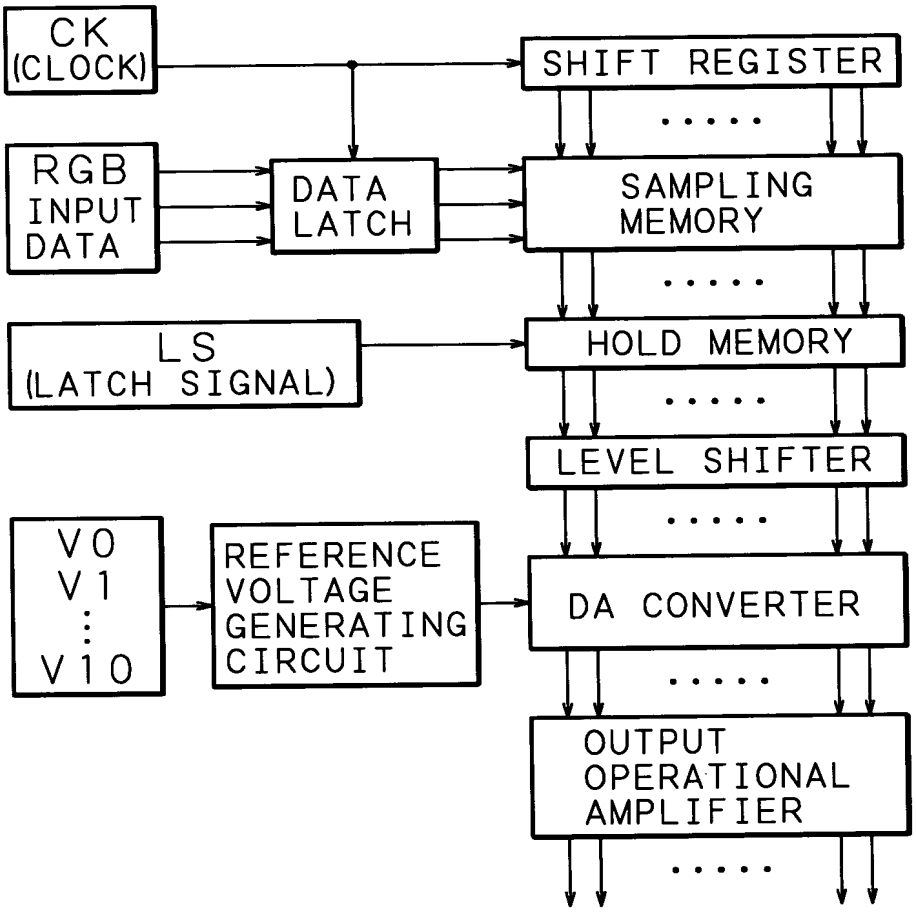


FIG. 18
PRIOR ART

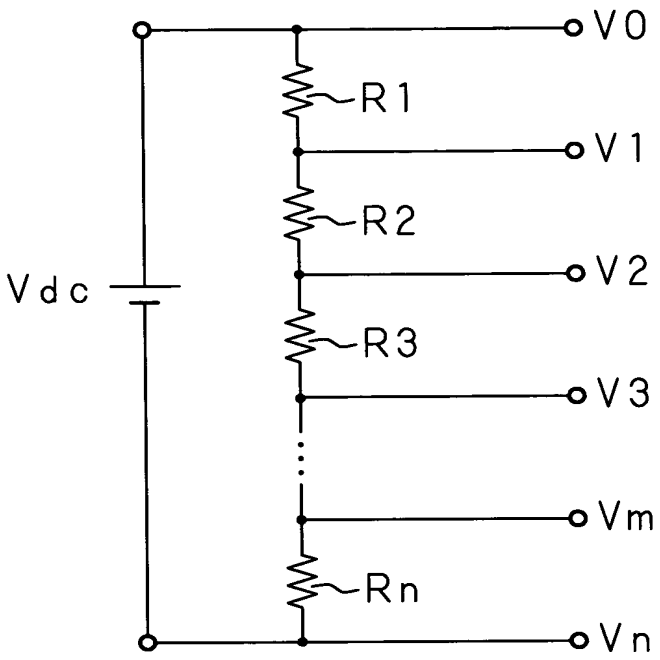


FIG. 19
PRIOR ART

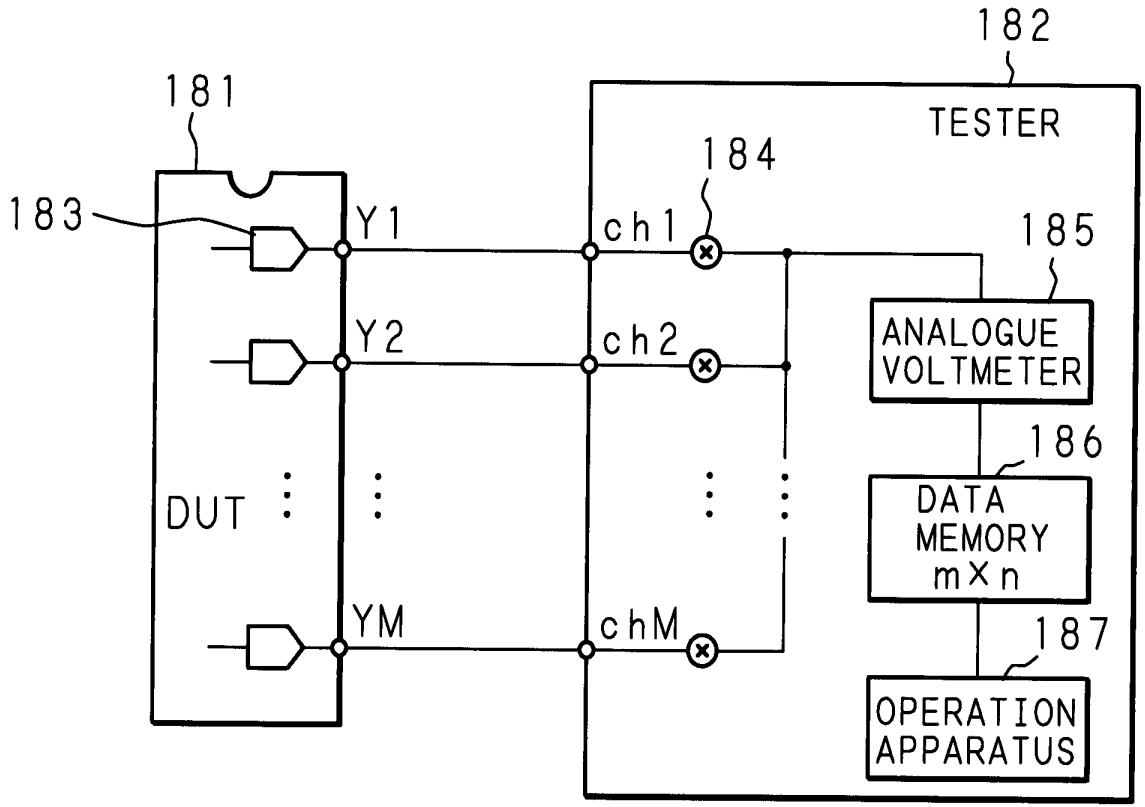
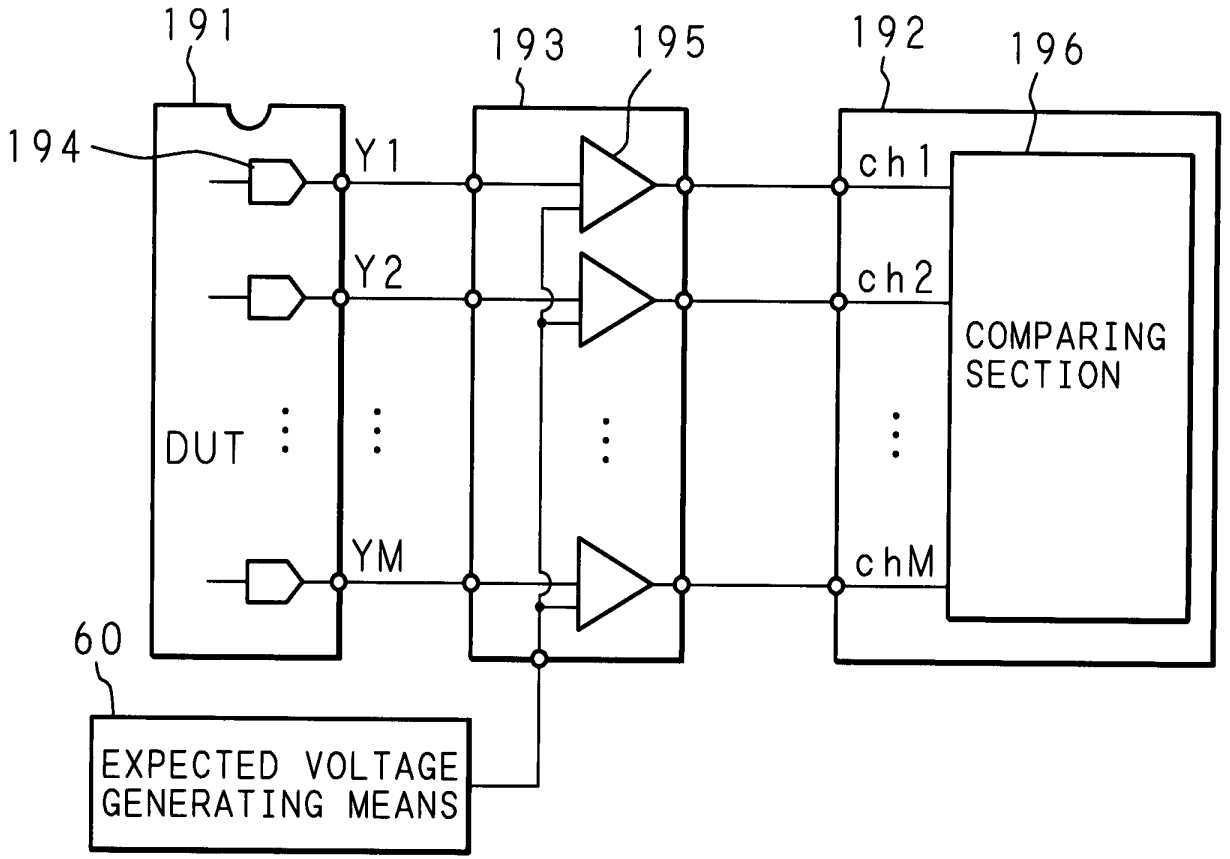


FIG. 20
PRIOR ART



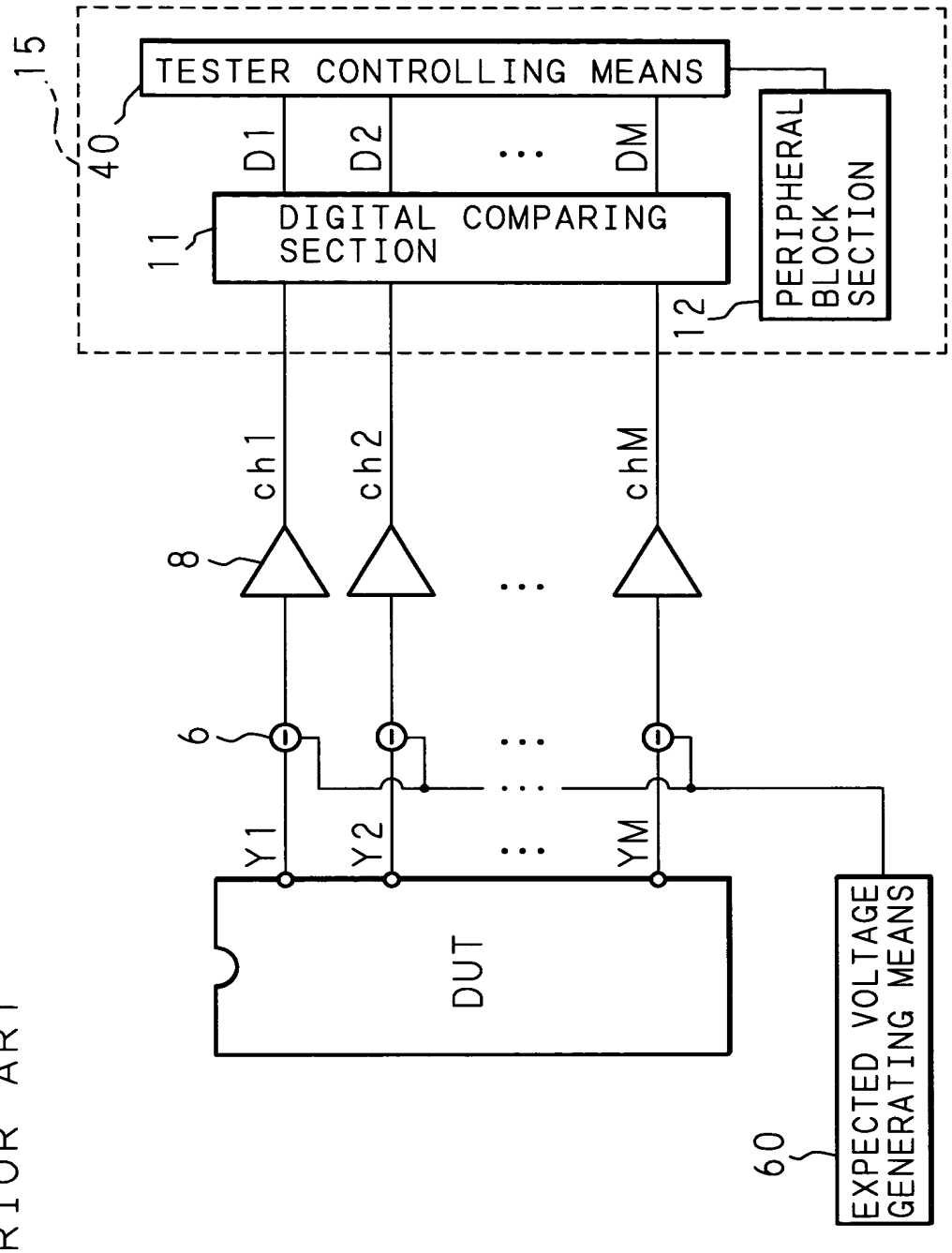


FIG. 21
PRIOR ART

FIG. 22
PRIOR ART

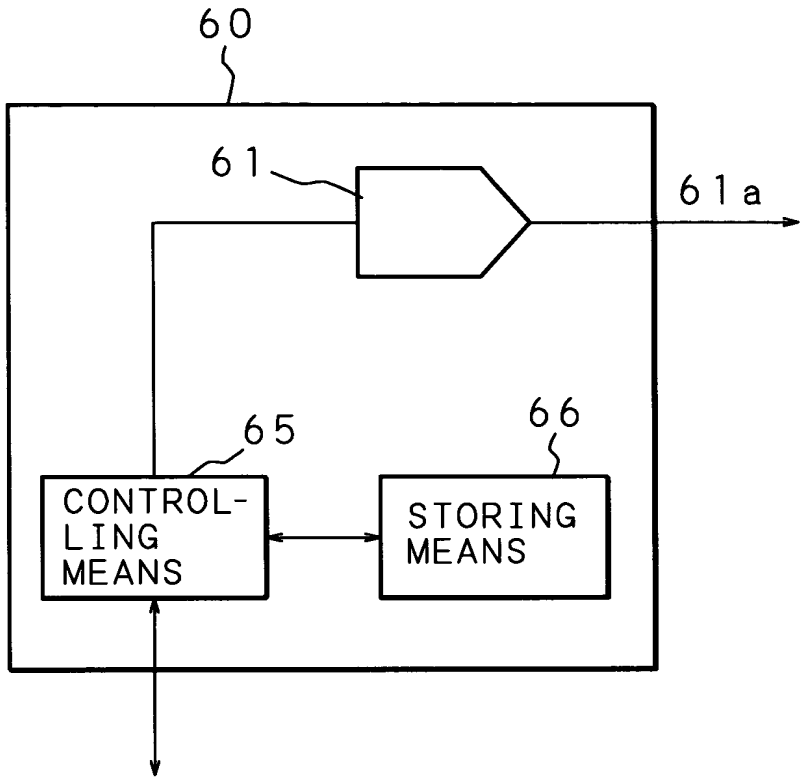
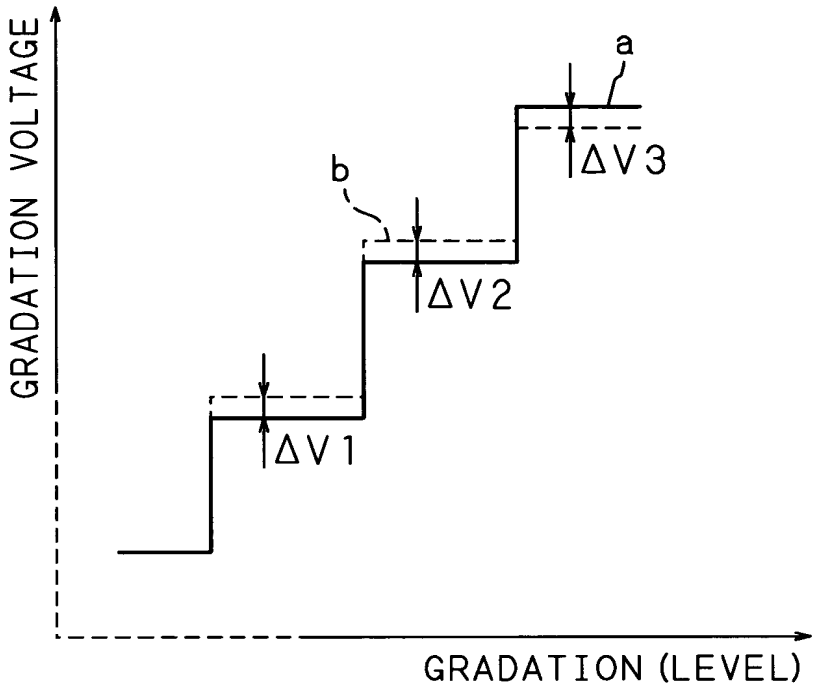


FIG. 23



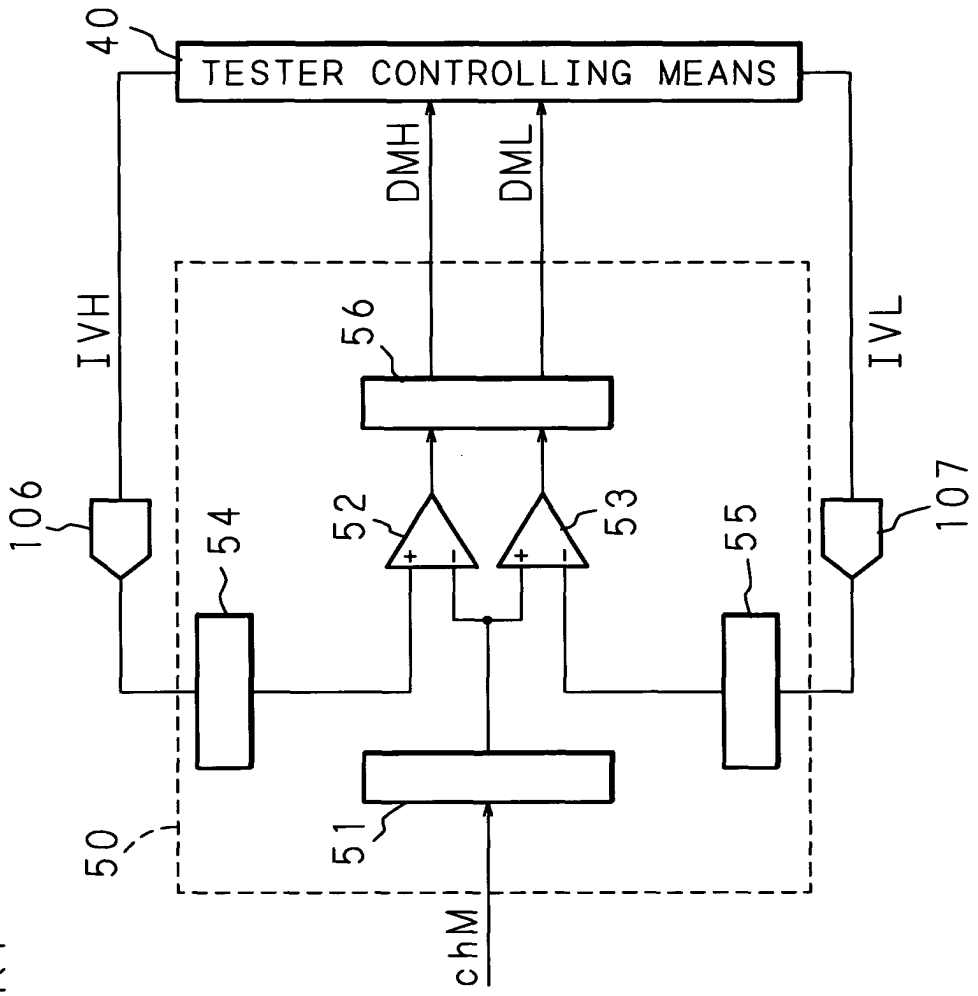


FIG. 24
PRIOR ART